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RN-8063

B. E. - II (Sem. III) (Computer) Examination

May / June – 2010

Computer Organization & Architecture

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 2 (Sem. 3) (Computer)**

Name of the Subject :

☛ **Computer Organization & Architecture**

☛ Subject Code No. : **8 0 6 3** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Draw flowchart or Block diagram wherever it is necessary.

(3) Make necessary asumption if required.

SECTION - I

1 (a) Answer the following : **10**

(i) What is computer Architecture?

(ii) A more efficient scheme for transferring information in a system with many registers is to use a common bus system. (True/False)

(iii) What is overflow in signed binary numbers?

(iv) Let A and B are Two signed numbers. A = 11110000 and B = 00010100. Perform A – B.

(v) What will be the values of Overflow Flag (V) and Zero Flag (Z) in above example.

(vi) What is Supervisor Mode?

Convert the following infix statements to reverse polish notation.

(vii) A * B + C * D – E

(viii) [A – B/C] * D + E

(ix) The way the operands are chosen during program execution is dependent on the _____ of the instruction.

(x) With logical operation can be used to selectively clear particular bits of register contents? Give examples.

(b) Explain first pass of the assembler. **6**

(c) What is Mapping of instruction? Explain it with example. **4**

2 (a) A two-word instruction is store in memory at an address designated by the symbol W. The address field of the instruction (stored at W+1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses. If addressing mode of the instruction is **8**

(a) Direct

(b) Indirect

(c) Relative

(d) Indexed

OR

(a) Explain stack organization with necessary micro operation. **8**

(b) Explain with Block Diagram, Decoding of micro operation fields. **6**

OR

(b) Assume that the control memory is 12 bit wide. The control portion of the microinstruction format is divided into two fields. A micro-operation field of 13 bits specifies the micro-operations to be performed. An address selection field specifies a condition, based on the flags that will cause a microinstruction branch. There are eight flags. **6**

(i) How many bits are in the address selection field?

(ii) How many bits are in the address field?

(iii) What is the size of the control memory?

3 Attmept any **four** : **16**

(i) The 4-bit adder-subtractor circuit has the following values for input mode M and data inputs A and B. In each case, determine the values of the outputs : S_3, S_2, S_1, S_0 and C_4.

s	M	A	B
a	0	0111	0110
b	0	1000	1001
c	1	1100	1000
d	1	0101	1010
e	1	0000	0001

(ii) Explain common bus system for four registers using multiplexers.

(iii) Write an assembly language program to add two double precision numbers.

(iv) Explain Status Register of the ALU.

(v) Explain CISC characteristics and compare it with RISC.

SECTION - II

4 (a) Do as directed : **10**

(i) Explain BSA instruction

(ii) Define effective address with proper demonstration.

(iii) Explain divide overflow.

(iv) Why should the sign of the reminder should be same as the sign of dividend after a division?

(v) Write down the applications of Supercomputer.

(b) Derive speed up $S = t_n / t_p$ and draw space time diagram for four segment pipeline. 8

5	(a)	Explain Array Processors.	8
		OR	
	(a)	Explain Data Dependency and Handling of branch instruction in instruction pipeline.	8
	(b)	Explain Booth's algorithm.	8
6	(a)	Give the difference between Hardwired Control Organization and Micro programmed Control Organization and draw the block diagram of basic computer.	8
	(b)	Explain and draw the flowchart for instruction cycle.	8
		OR	
	(b)	Explain the flowchart algorithm for adding and subtracting of two floating point numbers.	8